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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete If Known

Application Number	10/037,861
Filing Date	January 2, 2002
First Named Inventor	Chong, Yan
Group Art Unit	2151
Examiner Name	Unassigned
Attorney Docket Number	015114-054810

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U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
<i>[Signature]</i>	AA	5,555,214		Sung et al.	09-10-1996	
<i>[Signature]</i>	AB	5,633,830		Sung et al.	05-27-1997	
<i>[Signature]</i>	AC	5,764,080		Huang et al.	06-09-1998	
<i>[Signature]</i>	AD	5,802,540		Sung et al.	09-01-1998	
<i>[Signature]</i>	AE	5,828,229		Cliff et al.	10-27-1998	
<i>[Signature]</i>	AF	5,970,255		Tran et al.	10-19-1999	
<i>[Signature]</i>	AG	6,011,744		Sampla et al.	01-04-2000	
<i>[Signature]</i>	AH	6,049,255		Hagberg et al.	04-11-2000	
<i>[Signature]</i>	AI	6,100,713		Kalb et al.	08-08-2000	
<i>[Signature]</i>	AJ	6,128,692		Sung et al.	10-03-2000	
<i>[Signature]</i>	AK	6,147,520		Kothandaraman et al.	11-14-2000	
<i>[Signature]</i>	AL	6,236,231		Nguyen et al.	05-22-2001	
<i>[Signature]</i>	AM	6,252,419		Sung et al.	06-26-2001	

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>[Signature]</i>	AN	MICHAEL B. BENDAK et al., "CMOS VLSI Implementation of Gigabyte/Second Computer Network Links", IEEE, 1996, pp. 269-272	
<i>[Signature]</i>	AO	"Virtex-II 1.5V Field-Programmable Gate Arrays", XILINX, DS031-2 (v1.5), April 2, 2001, pp. 1-36	
<i>[Signature]</i>	AP	ANDREA BONI et al., "LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-μm CMOS" IEEE Journal of Solid-State Circuits, vol. 36, no. 4, April 2001, pp. 706-711	
<i>[Signature]</i>	AQ	"APEX II Programmable Logic Device Family", Altera Corporation, May 2001, pp. 1-8, 38-59	
<i>[Signature]</i>	AR	"APEX 20K Programmable Logic Device Family", Altera Corporation, May 2001, pp. 1-8, 37-47	

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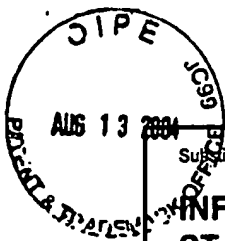
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		Art Unit	2151		
		Examiner Name	Thomas C. Lee		
Sheet	1	of	1	Attorney Docket Number	015114-054810US

U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. ¹	Document Number Number Kind Code ² (# known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	US-6,279,073	08-21-2001	McCracken et al.	RECEIVED AUG 18 2004
	AB	US-6,472,904	10-29-2002	Andrews et al.	
	AC	US-6,504,790	01-07-2003	Wolford	
	AD	US-			
	AE	US-			

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FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		Country Code ³	Number ⁴	Kind Code ⁵ (# known)				
	AF							<input type="checkbox"/>
	AG							<input type="checkbox"/>
NON PATENT LITERATURE DOCUMENTS								
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.						T ²
	AH							
	AI							
	AJ							

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